



A cross-sectional diagram of a semiconductor device. The structure consists of a central P-type region (labeled 'P') surrounded by N-type regions (labeled 'N'). These N-type regions are situated on a substrate that contains N⁺ regions (labeled 'N⁺'). The device is divided into several layers, indicated by numbers 1 through 6 on the left side. Layer 1 is the bottom-most N⁺ region. Layer 2 is the N-type region above it. Layer 3 is the N-type region surrounding the central P-region. Layer 4 is the P-type region. Layer 5 is the bottom-most N⁺ region. Layer 6 is the top-most N-type region. A central electrode is connected to the P-region, and side electrodes are connected to the N-regions.

[illegible]

PRIOR ART

Fig 2